CLAIM AMENDMENTS

Please amend the claims as described below. In accordance with 37 CFR §1.121, a complete listing of all claims in the application is provided below. Notably, the status of each claim is indicated in the parenthetical expression adjacent to the corresponding claim number.

1. (**Currently Amended**) A semiconductor memory array, comprising:

a plurality of semiconductor dynamic random access memory cells arranged in a matrix of rows and columns, each semiconductor dynamic random access memory cell includes at least one transistor having:

a source region;

a drain region;

a body region disposed between ~~and adjacent to~~ the source region and the drain region, wherein the body region is electrically floating; and

a gate spaced apart from, and capacitively coupled to, the body region;

wherein each memory cell ~~transistor~~ includes (1) a first data state which corresponds to ~~representative of~~ a first charge in the body region of the transistor of the memory cell, and (2) a second data state which corresponds to ~~representative of~~ a second charge in the body region of the transistor of the memory cell; and

wherein the source region of the transistor of each memory cell corresponding to a first ~~each~~ row of semiconductor dynamic random access memory cells is connected to the same ~~includes an associated~~ source line ~~which is connected to only the semiconductor dynamic random access memory cells of the associated row~~ and wherein the gate of the

transistor of each memory cell corresponding to the first row of semiconductor dynamic random access memory cells is connected to the same word line.

2. **(Currently Amended)** The semiconductor memory array of claim 1 wherein the drain region of the transistor of each memory cell of ~~each~~ the first row of semiconductor dynamic random access memory cells ~~includes~~ is connected to a ~~separate~~ different bit line ~~which is connected to the drain region of the associated transistor~~.

3. **(Currently Amended)** The semiconductor memory array of claim 2 wherein each memory cell of a the first row is programmed to a the first data state by applying a control signal, having a first amplitude, to the gate of the transistor of each memory cell of the first row and a control signal, having a second amplitude, to the drain region of the transistor of each memory cell of the first row.

4. **(Currently Amended)** The semiconductor memory array of claim 3 wherein a predetermined memory cell of the first row is programmed to a second data state by applying (1) a control signal, having a third amplitude, to the gate of the transistor of the predetermined memory cell, (2) a control signal, having an fourth amplitude, to the drain region of the transistor of predetermined memory cell, and (3) a control signal, having a fifth amplitude, to the source region of the transistor of predetermined memory cell of the first row.

5. **(Currently Amended)** The semiconductor memory array of claim 4 wherein an unselected memory cell of the first row is maintained in the first data state, while the predetermined memory cell is programmed to ~~a~~ the second data state, by applying a control signal, having ~~a~~ the third amplitude, to the gate of the transistor of the ~~predetermined~~ unselected memory cell and a control signal, having ~~an~~ sixth amplitude, to the drain region of the transistor of ~~predetermined~~ the unselected memory cell.

6. **(Currently Amended)** The semiconductor memory array of claim 5 wherein ~~all of~~ the predetermined memory cells ~~of the first row are~~ is read by applying a control signal, having a seventh amplitude, to the gate of the transistor of the predetermined memory cell and a control signal, having an eight amplitude, to the drain region of the transistor of predetermined memory cell.

7. **(Currently Amended)** The semiconductor memory array of claim 6 wherein all of the memory cells of a second row are maintained in an inhibit state while the predetermined memory cells of the first row is ~~are~~ read.

8. **(Currently Amended)** The semiconductor memory array of claim 6 wherein all of the memory cells of a second row are maintained in an inhibit state while the predetermined memory cells of the first row is ~~are~~ read by applying a control signal, having a ninth amplitude, to the gate of each ~~the~~ transistors of the memory cells of the second row.

9. **(Currently Amended)** The semiconductor memory array of claim 1 wherein the transistor of each memory cell of a the first row of semiconductor dynamic random access memory cells shares a drain region with a transistor of an adjacent memory cell ~~in~~ of a second row of semiconductor dynamic random access memory cells, wherein the first and second rows of memory cells are adjacent rows.

10. **(Currently Amended)** The semiconductor memory array of claim ~~9~~1 wherein ~~each~~ the gate of the transistor of each memory cell of a the ~~first~~ second row of semiconductor dynamic random access memory cells is connected to a ~~first~~ second ~~gate~~ word line.

11. **(Currently Amended)** The semiconductor memory array of claim 10 wherein the source region of the transistor of each memory cell of the second row of semiconductor dynamic random access memory cells is connected to a common source line ~~only the gate of each memory cell of the first row of semiconductor dynamic random access memory cells is connected to the first gate line~~.

12. **(Currently Amended)** A semiconductor memory array, comprising:

a plurality of semiconductor dynamic random access memory cells arranged in a matrix of rows and columns, each semiconductor dynamic random access memory cell includes at least one transistor having:

a source region;

a drain region;

a body region disposed between ~~and adjacent to~~ the source region and the drain region, wherein the body region is electrically floating; and

a gate spaced apart from, and capacitively coupled to, the body region;

wherein each transistor includes a first state representative of a first charge in the body region, and a second data state representative of a second charge in the body region;

wherein the source region of the transistor of each memory cell corresponding to ~~each~~ a first row of semiconductor dynamic random access memory cells is connected to a first ~~includes (1) an associated~~ source line ~~which is connected to only the semiconductor dynamic random access memory cells in the associated row~~ and ~~(2) a different~~ wherein the gate ~~line for~~ of the transistor of each memory cell corresponding to the first row of ~~each~~ semiconductor dynamic random access memory cells ~~in the associated row~~ is connected to a first word line;

wherein the source region of the transistor of each memory cell corresponding to a second row of semiconductor dynamic random access memory cells is connected to a second source line and wherein the gate of the transistor of each memory cell corresponding to the second row of semiconductor dynamic random access memory cells is connected to a second word line; and

wherein the first and second rows of semiconductor dynamic random access memory cells are adjacent rows.

13. **(Currently Amended)** The semiconductor memory array of claim 12 wherein the drain region of the transistor of each memory cell of ~~each~~ the first row of semiconductor

dynamic random access memory cells ~~includes~~ is connected to a ~~separate~~ different bit line ~~which is connected to the drain region of the associated transistor~~.

14. **(Currently Amended)** The semiconductor memory array of claim 13 wherein each memory cell of ~~a~~ the first row is programmed to a first data state by applying a control signal, having a first amplitude, to the gate of the transistor of each memory cell of the first row and a control signal, having a second amplitude, to the drain region of the transistor of each memory cell of the first row.

15. **(Currently Amended)** The semiconductor memory array of claim 14 wherein a predetermined memory cell of the first row is programmed to a second data state by applying a control signal, having a third amplitude, to the gate of the transistor of the predetermined memory cell, a control signal, having an fourth amplitude, to the drain region of the transistor of the predetermined memory cell, and a control signal, having a fifth amplitude, to the source region of the transistor of the predetermined memory cell of the first row.

16. **(Currently Amended)** The semiconductor memory array of claim 15 wherein an unselected memory cell of the first row is maintained in the first data state, while the predetermined memory cell is programmed to ~~a~~ the second data state, by applying a control signal, having a third amplitude, to the gate of the transistor of the unselected ~~predetermined~~ memory cell and a control signal, having an sixth amplitude, to the drain region of the transistor of the unselected ~~predetermined~~ memory cell.

17. (**Currently Amended**) The semiconductor memory array of claim 16 wherein all of the memory cells of the first row are read by applying a control signal, having a seventh amplitude, to the gate of the transistor of ~~the predetermined~~ each memory cell of the first row, and a control signal, having an eight amplitude, to the drain region of the transistor of each ~~predetermined~~ memory cell of the first row.

18. (**Currently Amended**) The semiconductor memory array of claim 17 wherein all of the memory cells of ~~a~~ the second row are maintained in an inhibit state while the memory cells of the first row are read.

19. (**Currently Amended**) The semiconductor memory array of claim 17 wherein all of the memory cells of ~~a~~ the second row are maintained in an inhibit state while the memory cells of the first row are read by applying a control signal having a ninth amplitude to the gate of the transistors of each ~~the~~ memory cells of the second row.

20. (**Currently Amended**) The semiconductor memory array of claim 12 wherein the transistor of each memory cell of ~~a~~ the first row of semiconductor dynamic random access memory cells shares a drain region with the transistor of an adjacent memory cell in ~~a~~ the second row of semiconductor dynamic random access memory cells~~, wherein the first and second rows of memory cells are adjacent rows~~.